THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: MATHEW, LEO, et al.	§	**Patent No.:** 6951783 B2
	§	
	§	**Issue Date:** 10-04-2005
Application No.: 10/695163	§	
	§	**Examiner:** Trung Dang
Filed: 10-28-2003	§	
	§	**Group Art Unit:** 2823
Docket No.: SC12746TP	§	
	§	

Title: CONFINED SPACERS FOR DOUBLE GATE TRANSISTOR SEMICONDUCTOR FABRICATION PROCESS

Certificate of Submission

I hereby certify that this correspondence is being submitted to the USPTO, Alexandria, VA.

☐ Addressed per C.F.R. § 1.1(a) and deposited with the United States Postal Service with sufficient postage as first class mail.

☐ Facsimile transmitted in accordance with C.F.R. §1.6(d).

☒ Submitted electronically via EFS in accordance with "Legal Framework for EFS Web".

2-11-08
Date of Submission

Pat Thomas
Signature

PAT THOMAS
Printed Name of Person Signing Certificate

Commissioner for Patents
Alexandria, VA 22313

SUBMISSION OF CERTIFICATE OF CORRECTION

Dear Commissioner:

Enclosed is a Certificate of Correction listing error(s) in the subject patent. Please enter these corrections. Since the errors appear to be on the part of the United States Patent Office, there should be no charge.

Respectfully submitted,

2008-02-08
Date

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SC12746TP

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Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.:	6951783 B2
APPLICATION NO:	10/695163
DATE:	10-28-2003
FIRST NAMED INVENTOR:	MATHEW, LEO

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In Column 8, Line 64, Claim No. 16:

Change "overlaying" to –overlying—

In Column 9, Line 5, Claim No. 16:

Change "within fin underlying" to -- within the silicon fin underlying--

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